UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,942	04/13/2000	Warren M. Farnworth	4161US (98-1265)	6934

7590 04/26/2004

Joseph A Walkowski
Trask Britt & Rossa
P O Box 2550
Salt Lake City, UT 84110

EXAMINER	
LEE, BENNY T	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 04/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER NUMBER

DATE MAILED:

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on 5 July 2000 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire three (3) month(s), ~~_____~~ days from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☒ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-22 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☒ Claims 1-9; 10-12; 13 & 14; 15-18; 19; 20, 21, & 22 are rejected.

5. ☐ Claims _____ are objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.

8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).

10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW TO EFFECT DRAWING CHANGES", PTO-1474.

12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.

13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

TOL-326 (Rev. 7-82) EXAMINER'S ACTION

SN 548942

1. The disclosure is objected to because of the following informalities: Page 2, line 29 and page 3, line 27, not that "Sep" should be rephrased as – issued September – at each occurrence for clarity of description. Page 3, line 7, note that "jul should be rephrased as issued July – for clarity of description. Page 3, line 30 and page 4, line 4, note that "Dec" should be rephrased as – issued December – at each occurrence for clarity of description. Page 4, line 8, note that "Aug". should be rephrased as – issued August – for clarity of description. Page 5, line 20, note that "OF THE SEVERAL VIEWS" should be deleted as being unnecessary. Page 9, line 1, should "substrate" correctly be – substrate – for consistency with figure 8"? line 2, note that -- adjacent -- should follow "two" for clarity of description; line 6, note that "21" should follow "second surface" for consistency with "figure 8". Page 10, line 8, note that – (see fig. 13) – should follow "40" for consistency with "figure 13". Page 10, line 30 and page 11, line 14, note that – (PCB) – should precede each occurrence of "106" for consistency with figure 14. Page 11, line 15, note that – respective should precede "cache" for clarity of description. Note that reference labels (4, 6) appearing in figure 2 needs a corresponding reference in the specification's description of figure 2. Similarly reference label "12" appearing in "figure 4" needs a corresponding reference in the specification's description of "figure 4".

Appropriate correction is required.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the passivation layer

(i.e. cls 6, 14, 17)) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claims 2, 6, 8, 9, 11, 12, 20, 21, 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 2, 6, note that it is unclear how "at least one of the conductive trace layers" (e.g. same as different from, etc). Clarification is needed. relate to each other in these claims

In claim 8, note that it is unclear how "at least one of the at least two conductive trace layers" relates to the same recitation already recited din claim 1 (e.g. same as, different from, etc). Clarification is needed.

~~In claim 8, note that it is unclear how at least one of the at least two conductive trace layers relates to the same recitation already recited in claim 1 (e.g. same as different from etc). Clarification is needed.~~

In claims 9, 20, note that it is unclear which "traces" are intended as recited.

In claim 11, note that it is unclear whether the "at least one electrically conductive layer" (being the at least one signal trace in cl. 10) can be properly characterized as being "comprised in the voltage reference portion". Clarification is needed.

In claim 12, note that it is unclear whether "the voltage reference bus" and "traces extending therefrom" can properly depend from a claim where the voltage reference portion has "a greater surface area than the at least one signal trace".

Clarification is needed.

In claims 20, 22, note that it is unclear what characterizes "at least one component of the electronic system" (i.e. the processor, one or more of the devices, etc). Clarification is needed.

The following claim have been found objectionable for reasons set forth below:

In claim 2, note that "its length" should be rephrased as --the length thereof --.

In claim 3, note that – insulative layer – should follow "each".

In claim 21, note that "to its extent" should be deleted as being unnecessary.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, 9, 10, 11, 15, 16, 18, 19 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kobayashi et al.

Kobayashi et al discloses a printed circuit board arrangement comprising at least one substrate layer. Note that a plurality of conductive signal layers or traces (e.g.

112a, 112b, 112c) separated by ground areas or traces (114) disposed on the same surface as the conductive signal layers. The ground areas or traces (114) serve as a voltage reference (i.e. ground) and include via hole connections (115) which electrically connect traces (114) to a ground or voltage reference plane 113. As is evident from fig. 4, the signal traces (e.g. 112a, 112b, 112c) have a change in direction (i.e. a slanted portion). As evident from the alternate embodiment (e.g. fig. 10), there are alternating dielectric and conductive layers where each conductive layer has signal traces (e.g. 125) separated by ground traces (e.g. 127). Furthermore, as evident from fig. 4, the voltage reference ground area traces (114) has a greater surface area than the co-planar signal traces (i.e. 112a, 112b, 112c).

Claims 1, 3-5, 15, 16,18, 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by the East German reference.

The East German reference discloses a printed circuit board having alternating insulating layers (Er) and conductive tracks or trace layers. The conductive trace layers include signal lines or conductive traces (1) with voltage reference (i.e. ground) lines or traces (2) interposed across a gap or trough between adjacent signal traces (1) in each conductive trace layer. Moreover, it is evident that the voltage reference (i.e. ground) traces (2) have a greater surface area than the signal traces (1).. As is evident from the alternate embodiment in fig. 4, one of the conductive layer (i.e. signal and voltage reference traces) is inherently electrically coupled thereto through the interposing insulating layer.

Claims 1, 8, 9, 13 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hoffman.

Hoffman (figs. 1A, 1B) discloses a printed circuit board comprising a plurality of parallel signal conductors (e.g. 18) disposed on opposite surfaces thereof. Moreover, a plurality of parallel voltage reference (i.e. ground) conductors or traces (20/1, 20/2, ...) extend from and electrically connected to a common conducting area or voltage reference bus (e.g. 19) disposed along an edge (14) of the printed circuit board to provide shielding between signal conductors (18). ~~As evident from fig. 2, conductive vias (47) electrically connect voltage reference (e.g. 19) disposed along an edge (14) of the printed circuit board.~~ As evident from fig. 2, conductive vias (47) electrically connect voltage reference traces on the opposite sides of the printed circuit board.

Claims 1, 2, 10, 11, 15, 16, 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Wakeling.

Wakeling (Figs. 1, 2,) discloses a printed circuit board comprising an insulating board (12) and conductive track or trace layers (14) disposed on opposite surfaces of the insulating board (12). As evidence from fig. 1, the conductive trace layers (14) includes parallel signal traces or traces (14a) and voltage reference (i.e. ground) tracks or traces across troughs to electrically isolate and shield the adjacent signal traces. Also, as is evident from fig. 1, the signal traces have a direction change at lateral portion (34) while the voltage reference tracks comprises the majority of the conductive layer and is comprised of a continuous conductive layer whose surface area is greater than the surface area of any one signal trace.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al or Wakeling in view of Forbes et al.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffman in view of Forbes et al.

Note that each of the printed circuit boards of the above cited primary references includes at least one conductive trace layer which is exposed to the external environment.

Forbes et al (fig. 2) discloses a printed circuit board having a conductive trace layer (240, 250, 240B) in part functions to isolate the conductive trace layer from the external environment.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have added insulating layers to cover otherwise exposed conductive layers on surfaces of the printed circuit board as taught by Forbes et al.

Such a modification would have provided the advantageous benefit of isolating and protecting the conductive traces from the detrimental effects of exposure to the external environment.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al in view of either Kobayashi et al or Wakeling.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al in view of either Kobayashi et al or Wakeling.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al in view of either Wakeling or the East German reference.

Forbes (Fig. 10) discloses an electronic system (1000) comprising a processor (1020) electrically connected by a bus to an integrated circuit (1010). As described at col. 5 ls 31-33 and col. 5 ls 46-49, the integrated circuit may be comprised as a memory module (e.g. a DRAM). Moreover, as known to those of ordinary skill in the art, processor (e.g computer processors) are known to inherently include input/output devices, data storage devices, et c associated therewith.

Accordingly, in view of the generic nature of the bus in Forbes et al it would have been obvious that any equivalent bus arrangement (e.g. as in any one of the above secondary references) would have been usable therein and yet retain the function of the bus in the electronic system of Forbes et al. Regarding claim 21, note that as an obvious consequence of the combination with Wakeling or Kobayashi et al non-linear conductive e.g. slanted lateral etc) paths result. Regarding claim 22, note that as an obvious consequence of the combination with Wakeling or the East German reference, the voltage reference (i.e. ground) plane or layer is greater in surface area than any one signal conductor or trace.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Compton (Fig. 6) discloses parallel signal conductors (S) shield by ground conductors (G). Millar is a bus with shielded conductors.

Any inquiry concerning this communication should be directed to Benny T Lee at telephone number (571)272-1764.

Benny Lee

BENNY T. LEE
PRIMARY EXAMINER
ART UNIT 2817